REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 15, 19 and 38-66 are in this application. Claims 15, 40, 45, and 51-53 have been amended. Claims 57-66 have been added to additionally and alternately claim the present invention.

The Examiner rejected claims 15, 19, 38-39, and 45-56 under 35 U.S.C. §112, first paragraph. With respect to claims 15, 19, 38-39, and 45-50, the Examiner noted that applicant's FIG. 16 depicts a plurality of positive lines that are connected to pads via ESD switches. The Examiner also noted that the positive lines shown in applicant's FIG. 16 are not directly connected to the pads. The Examiner argued, however, that there is no support in the specification for a claim that recites that none of the positive lines are connected to pads.

Although applicant disagrees with the Examiner's argument as previously set forth in applicant's amendment dated May 7, 2002, to further prosecution, applicant has amended claim 15 to recite, as noted by the Examiner, that the positive lines are not directly connected to the pads. Thus, claim 15 is believed to satisfy the requirements of the first paragraph of section 112. In addition, since claims 19, 38-39, and 45-50 either directly or indirectly depend from claim 15, claims 19, 38-39, and 45-50 are believed to satisfy the requirements of the first paragraph of section 112 for the same reasons as claim 15.

With respect to claim 45, the Examiner argued that the embodiment shown in applicant's FIG. 16 does not support a claim limitation of ESD positive lines never being connected to a steady voltage source. Applicant disagrees with the Examiner's argument for the same reasons as set forth with respect to claim 15. However, to further prosecution, applicant has amended claim 45 to recite that the ESD positive lines are never directly connected to a steady voltage source. As a result, claim 45 is believed to satisfy the requirements of the first paragraph of section 112.

With respect to claims 51-56, the Examiner argued that the embodiment shown in applicant's FIG. 16 does not support a claim limitation of a switch that has a reverse breakdown voltage that is less than the reverse breakdown voltage of the second diode. The

phrase cited by the Examiner has been removed from claim 51. As a result, claim 51 is believed to satisfy the requirements of the first paragraph of section 112. In addition, since claims 52-56 either directly or indirectly depend from claim 51, claims 52-56 are believed to satisfy the requirements of the first paragraph of section 112 for the same reasons as claim 51.

The Examiner also rejected claim 52 under 35 U.S.C. §112, second paragraph. Specifically, the Examiner argued that the claimed limitation of a positive line rising at a predetermined rate that is different from the predetermined rate is unclear. Applicant notes that claim 52 recites a voltage rising at a predefined rate that is different from the predetermined rate. However, to provide further clarity, applicant has amended claim 52 to recite a voltage rising at a second rate that is different from the first rate. Claims 51 and 53 has been similarly amended.

In addition, applicant notes that applicant's FIG. 16 shows a plurality of ESD switches 1625, such as ESD switch 130 shown in applicant's prior art FIG. 2. (See applicant's specification page 34, lines 1-2.) The operation of prior art ESD switch 130 shown in applicant's FIG. 2 is based on the rate of change of the voltage on line 120. When an ESD event occurs, the voltage on line 120 changes quickly and, as a result, has a high rate of change.

However, because of the resistor and capacitor, the voltage on the gate of PMOS transistor 220 shown in applicant's FIG. 2 lags behind the voltage on line 120. As a result, the gate voltage falls below the source voltage on line 120 a sufficient amount to turn on PMOS transistor 220. When PMOS transistor 220 turns on, transistor 220 charges up the voltage on the gate of NMOS transistor 210, thereby turning on transistor 210 to provide the ESD protection.

On the other hand, during a standard power up sequence, the voltage on line 120 rises much slower than when an ESD spike is present and, as a result, has a slower rate of change. The voltage on the gate of PMOS transistor 220 lags behind the voltage on line 120, but the lag is insufficient. As a result, the gate voltage does not fall below the source voltage on line

120 by enough to turn on PMOS transistor 220. In this case, NMOS transistor 210 remains turned off.

Thus, the "first rate" of claims 51 and 53 can be read to be the rate of change of the voltage on line 120 when an ESD event occurs, while the "second rate" of claim 52 can be read to be the rate of change of the voltage on line 120 when the system is powered up. As a result, it is believed that claim 52 satisfies the requirements of the second paragraph of section 112.

The Examiner rejected claims 15, 19, 38-39, and 45-56 under 35 U.S.C. §103(a) as being unpatentable over Gens et al. (U.S. Patent No. 6,055,268) in view of the Admitted Prior Art (APA). For the reasons set forth below, applicant respectfully traverse this rejection.

Claim 15 recites, in part,

> "a plurality of pads; [and]
> "a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad. [Brackets added.]

In rejecting the claims, the Examiner pointed to pads P1 and P2 shown in FIG. 2 of Gens as constituting the plurality of pads, and the horizontal lines connected to the right side of the high-power supply terminals labeled VDD1 and VDD2 as being the plurality of positive lines in Gen's structure.

In the amendment filed on May 7, 2002, applicant noted that the Gens reference expressly teaches that the boxes P1, P2, VDD1, VDD2, VSS1, and VSS2 are pads. (Boxes P1 and P2 are I/O pads, boxes VDD1 and VDD2 are power supply pads, and boxes VSS1 and VSS2 are ground pads.) In addition, since the horizontal lines are directly connected to boxes VDD1 and VDD2, it is not possible for FIG. 2 of Gens to teach horizontal lines that are not directly connected to a pad.

In response, the Examiner noted that square blocks VDD1 and VDD2 provide power, and that the power is provided to the diodes via the horizontal lines. The Examiner then argued that, therefore, the horizontal lines are a plurality of ESD positive lines. Applicant respectfully does not understand the Examiner's argument. The statement that power is

provided to the diodes via the horizontal lines does not change the fact that the horizontal lines are connected to pads. This being the case, it is not possible for Gens to teach that the horizontal lines (identified by the Examiner as positive lines) are not directly connected to a pad.

The Examiner also argued that Gens teaches the claimed limitation of "none of the positive lines being connected to a pad" because the horizontal lines connected to boxes VDD1 and VDD2 are not connected to box P2. The Examiner's argument, however, fails for two reasons. First, the claim limitation requires that none of the positive lines be directly connected to a pad. As noted above, a horizontal line is directly connected to the VDD1 box which is a pad. Arguing that the horizontal line is not connected to another pad, pad P2 in this case, does not change the fact that the horizontal line is connected to a pad, which is all that the claim requires.

Second, the Examiner may not take inconsistent positions when interpreting claim terms. The Examiner argued that ESD positive lines 1640-1647 are connected to pads because ESD positive lines 1640-1647 are connected to pads via an intermediate structure, in this case diodes 1635. (See page 8, paragraph 11 of the June 25, 2002 office action.) The Examiner, however, may not then argue that the horizontal line connected to box VDD1 is not connected to box P2 because of an intermediate structure, in this case diodes D1 and D2.

In addition, although the Examiner argued that Gens teaches that none of the positive lines are connected to a pad, the Examiner also acknowledged the opposite position, that Gens does not teach that the plurality of positive lines are not connected to pads. (See page 6, line 4, of the June 25, 2002 office action.)

The Examiner also pointed to applicant's prior art FIGs. 1 and 2 as teaching a switch that is connected to a positive line, wherein the plurality of positive lines not being connected to pads. Although applicant's prior art FIG. 2 shows a transistor connected to line 120, FIG. 2 shows the transistor connected to only one line 120. As a result, applicant does not understand the Examiner's comment "wherein the plurality of positive lines not being connected to pads."

The Examiner continued by arguing that it would be obvious not to connect the horizontal line (read to be a positive line) to box VDD1 (which is a pad) to provide more effective unidirectional flow of current during an ESD event. Applicant respectfully does not understand the Examiner's argument. The Examiner appears to be arguing that one skilled in the art would be motivated to place a switch or a transistor between the box VDD1 and the horizontal line that is connected to box VDD1 to provide a more effective unidirectional flow of current during an ESD event. However, current flow during an ESD event must be bidirectional at the pad. Current must be able to flow out of the pad if the pad is positive during an ESD event, and must be able to flow into the pad if the pad is ground during an ESD event. As a result, one skilled in the art would not be motivated to place a switch between the VDD1 pad and the horizontal line to obtain better unidirectional current flow.

Thus, in view of the above, claim 15 is patentable over the Gens reference in view of the APA. In addition, since claims 19, 38-39, and 45-50 depend either directly or indirectly on claim 15, claims 19, 38-39, and 45-50 are patentable over Gens in view of the APA for the same reasons as claim 15..

With respect to independent claim 51, the Examiner argued that FIG. 2 of the APA teaches a reverse breakdown voltage of a switch 130 that is less than the reverse breakdown voltage of the second diode. As noted above, the phrase reciting the reverse breakdown voltage has been removed from claim 51. Applicant, however, can not find where the Examiner addressed applicant's argument regarding the patentability of claim 51 that applicant set forth in the amendment filed on May 7, 2002. As a result, applicant assumes that independent claim 51 is patentable over Gens in view of the APA. In addition, since claims 52-56 depend either directly or indirectly from claim 51, claims 52-56 are patentable over Gens in view of the APA for the same reasons as claim 51.

During a telephonic interview with the Examiner on September 18, 2002, applicant's attorney understood the Examiner to indicate that claims 40-44 would be allowable if rewritten in independent form to include the limitations of the base claim and any intervening claims. Claim 40 has been amended to be in independent form, and is believed to include all

of the relevant limitations of claim 15. Claims 41-44 have not been amended as these claims either directly or indirectly depend from claim 40.

During the telephonic interview, applicant's attorney also understood that claims 15 and 51 would be allowable if amended to recite that only one second diode is connected between a pad and a positive line. New claims 57 and 62 have been added, and are believed to recite the limitations suggested by the Examiner which would make claims 15 and 51, respectively, allowable. As a result, new claims 57 and 62 are believed to be allowable over Gens in view of the APA. In addition, since new claims 58-61 and new claims 63-66 depend either directly or indirectly from new claims 57 and 62, respectively, claims 58-61 and 63-66 are patentable for the same reasons as claims 57 and 62, respectively.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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APPENDIX

In the Claims

Please amend the claims as follows:

15. (Fifth Amendment) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring; and

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

40. (Amended) [The semiconductor chip of claim 15 wherein a first diode of the plurality of first diodes comprises:] A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring, a first diode of the plurality of first diodes including:

a plurality of first regions, the plurality of first regions being spaced apart from each other;

a second region, the plurality of first regions being formed in the second region, the plurality of first regions and the second region having opposite conductivity types, the second region having a dopant concentration; and

a third region formed in the second region, the third region being spaced apart from each first region, and formed between each adjacent pair of first regions, the third region having a dopant concentration that is higher than the dopant concentration of the second region; and

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

45. (Twice Amended) The chip of claim 15 wherein the ESD positive lines are never directly connected to a steady voltage source.

51. (Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch, a switch of the plurality of ESD switches passing a current from a positive line to the negative ring when a voltage on the positive line rises at a [predetermined] first rate;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring; and

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line [, a second diode having a reverse breakdown voltage,

the reverse breakdown voltage of a switch being less than the reverse breakdown voltage of the second diode].

52. (Amended) The chip of claim 51 wherein the switches block a current from flowing from the positive line to the negative ring when a voltage on the positive line rises at a [predefined] second rate that is different from the [predetermined] first rate.

53. (Amended) The chip of claim 51 wherein the second diodes are forward biased when the voltage on the positive line rises at the [predefined] second rate.

Claims 57-66 have been added.